REMARKS

In the Office Action dated 11/27/02 claims 9-17 were allowed. From the record it does not appear that the allowance was withdrawn, although a subsequent issue with respect to indefiniteness was raised in the Office Action of 0/10/03. These issues were addressed by amendment on 6/10/03. The proposed amendment was without detailed explanation refused entry as allegedly raising new issues requiring further search and consideration. Believing that the finding was in error at least as to claims 9-17 which had only minor amendments made thereto, Applicants filed an RCE to obtain further consideration. In response thereto and by Office Action dated 9/08/03, the prior formality rejections were acknowledged to have been overcome, but at this late date the claims including claims 9-17 were rejected as being obvious in view of a combination of three prior art references.

In the responsive Office Action mailed 5/05/04, the PA reference was dropped and the rejection essentially repeated.

Applicants respectfully traverse the rejection with respect to claims 9-17 now presented on the grounds that the principal reference TA is directed to a method and system for generating test patterns that are used for testing an IC device which is to be fabricated, recognizes that accurate test patterns are necessary to ensure proper operation of a fabricated IC device, and seeks to provide these accurate test patterns in an efficient and expedient fashion. However, rather than recreating these test patterns from the beginning after the device is fabricated, TA relies on the software simulation stage of the IC production process, and uses information available during the software simulation stage to create the test patterns, which can then be applied to the fabricated IC to determine proper operation. TA is particularly concerned with ensuring that the test patterns are valid and can provide an accurate assessment of the proper operation of the IC device, and uses a suitably configured evaluation system 20 to determine the validity of the generated test pattern. While a VCD file can be used to generate and evaluate the test pattern, there is no discussion in TA of the *selection* of a simulation session range, or of a target session range within the simulation session range. Moreover, the VCD file in TA is not used by the operator for debugging purposes, as in the case of the presently claimed invention, but is rather used for assembling and evaluating the test patterns which are to be applied to the fabricated IC. Since the test patterns are intended as a global tool for testing of the operation of the IC in virtually all conditions and with all combinations of inputs, there would be no value to selectively targeting ranges, and ranges within ranges, or to generating a

VCD file "dedicated to the state information in the selected simulation target range and being exclusive of state information outside said selected simulation target range," as is presently claimed. TA neither contemplates this type of approach, nor has any use for it.

Furthermore, in the Post-Simulation Analysis Mode section in cols. 41 and 42, LI discusses logging frequency in support of VCD, but only mentions that this frequency can be adjusted. There is no discussion of selection of simulation ranges, or target ranges, or of generating VCD files dedicated to the state information in the selected simulation target range and being exclusive of state information outside said selected simulation target range. Applicants request reconsideration of the rejection.

However, in order to advance prosecution of the subject application, Applicants have cancelled claims 1-8 and 18-22 and may represent same in a subsequent continuing application, and herein request reconsideration of the previously allowed claims 9-17 and the issuance of a notice of allowance with respect thereto.

Respectfully submitted,

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